UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/031,937	01/22/2002	Masataka Fukui	3552/0K216US0	8713

7590 08/23/2004

Darby & Darby
805 Third Avenue
New York, NY 10022

EXAMINER	
BAKER, STEPHEN M	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/031,937	FUKUI ET AL.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it is prolix and not in idiomatic English. Suggested corrections are provided below. Correction is required. See MPEP § 608.01(b).

> An object of the present invention is to provide an interleaver and a deinterleaver~~,~~ which are small-sized and power saving. An address converter ACON has three counters CNT1, CNT2 and CNT3 ~~in~~ associated with a first rank through a third rank and the outputs DO11, DO12 and DO13 of respective counters CNT1, CNT2 and CNT3 are ~~inputted in~~ input to lookup tables LUT1, LUT2 and LUT3. In the counter CNT3, a clock CK1 with a predetermined ~~cycle~~ rate is ~~inputted~~ input and the numeric values of "0" through "3" are repeatedly ~~outputted~~ output. In the counter CNT2, a carry out CO3 ~~to be outputted in synchronization with the output of~~ output from the counter CNT3~~, i.e., "0"~~ is ~~inputted~~ input as a clock CK2~~. Further~~, and the counter CNT2 outputs the numeric values of "0" through "4" repeatedly. In the counter CNT1, a carry out CO2 ~~to be outputted in synchronization with the~~ output of the counter CNT2~~, i.e., "0"~~ is ~~inputted~~ input as a clock CK3~~. Further~~, and the counter CNT1 outputs the numeric values of "0" through "15" repeatedly.

2. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are provided below, with suggested corrections:

> [0002] As a method for decreasing an effect of a noise against transmission data, ~~the~~ interleaving ~~is known where an~~ has been used whereby the order of ~~respective bits of~~ data bits is evenly ~~blended~~ rearranged and a ~~bit~~ row of reordered data bits is transmitted ~~after its order has been blended~~.
> At a receiving side, ~~the~~ deinterleaving is performed to return the ~~blended~~ reordered data to its original order so as to reproduce the data. Therefore, it is prevented that the ~~bit row is~~ bits of the originally ordered data are concentrated

together during one noise burst and deteriorated, so that it becomes easy to reproduce the data. Then, the longer the length of a data unit ~~for the data~~ to be ~~blended~~ reordered becomes, the more it is possible to decrease the effect of the noise burst. However, in order to perform ~~this~~ such interleaving and ~~this~~ deinterleaving, a lookup table to indicate a data ~~blending~~ reordering state is needed, and the longer the data unit to be ~~blended~~ reordered is, the larger the lookup table that is needed.

Appropriate correction is required.

3. The disclosure is objected to because of the following informalities:

Paragraph [0003] is incomprehensible.

Regarding the description [0042], [0043] of Figs. 1 and 2, "registers" DREG1 and DREG2 are each described as being capable of holding a "row" of data, and the addresses ADRC and ACON are apparently described as row addresses. A row apparently holds only 16 bits of data, according to Fig. 4. In apparent contrast, Fig. 3 suggests that ACON and ADRC include row and column addresses, that apparently can address any bit in an array of 320 bits (16 × 20). Fig. 4 shows half of the interleaving process as a 16-bit row reordering operation on a (16 × 20) array, but also shows a second half of the interleaving process as a 20-bit column reordering operation on the same array. Thus it appears that the sizes of DREG1 and DREG2 are apparently not disclosed correctly, or Figs. 1 (and 2) are incomplete arrangement for interleaving (and deinterleaving), each lacking at least additional storage for the remaining 19 rows. It appears most likely that DREG1 and DREG2 are each bit-addressable storage arrays and each has sufficient capacity to store the entire 16 × 20 bit array, and to decode the entire 9-bit address (ACON or ADRC) suggested by Fig. 3. The name "register" would in such case be misdescriptive, as would the designations DREG1 and DREG2.

Renaming registers DREG1 and DREG2 as arrays DARRAY1 and DARRAY2 would apparently correct the discrepancy. ACON and ADRC apparently should be described as bit addresses, not row addresses, in such case.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is misdescriptive, not in grammatical or idiomatic English, is elliptical in some parts and vague in others and lacks an essential element described in claim 2.

Claim 2 is elliptical and not in grammatical or idiomatic English.

In claims 4 and 5, "register" is considered needlessly confusing terminology for what is disclosed as a bit-addressable storage capable of holding at least 512 bits; "blending" is apparently unnecessarily non-standard terminology in the interleaving art.

Claims 1, 2, 4 and 5 apparently should be amended as follows:

1. An address converter comprising:

an upper rank lookup table to sequentially output, not more than m times, ~~pieces of elements equivalent to~~ a row address for a predetermined ~~line~~ row of a m × n matrix, said row address having ~~the number of the elements~~ not less than the ~~length of~~ number of elements in a ~~predetermined address data~~ row of said matrix;

a lower rank lookup table to sequentially and repeatedly output n ~~pieces of elements equivalent to said predetermined row~~ column addresses of said m × n matrix, not more than m times; and

an adder to add the output of said upper rank lookup table and a result using the output of said lower rank lookup table and output said ~~predetermined address data row~~ row and column addresses.

2. An address converter according to claim 1, wherein said address converter further comprises ~~with~~ a multiplier to multiply the output of the lower rank lookup table ~~with~~ by m and input ~~it in~~ the result to said adder ~~instead of directly inputting~~ as said result using the output of said lower rank lookup table ~~in said adder~~.

4. An interleaver comprising:
said address converter according to claim 1,
a first ~~register~~ storage to hold a data row to be ~~blended~~ reordered; and
a second ~~register~~ storage to ~~register a~~ hold the data row of said first register reordered ~~in an order of the blending address data row on the basis of said blending address data row~~ when an ~~initial address data row is inputted in~~ original row address is input to said address converter.

5. A deinterleaver comprising:
said address converter according to claim 1,
a second ~~register~~ storage to hold a data row to be ~~blended~~ reordered; and
a first ~~register~~ storage to ~~register~~ hold a data row of said second ~~register~~ storage in an original order ~~of the initial address data row on the basis of the blending address data row~~ when ~~said initial address data row is inputted in~~ an original row address is input to said address converter.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,625,234 to Cui *et al* ("Cui" hereafter).

Fig. 5 of Cui shows a de-interleaver including "an upper rank lookup table" (560), "a lower rank lookup table" (530), and "adder" (520), and a "multiplier" (500). Fig. 4B shows a corresponding interleaver.

Regarding claim 3 and 6, Cui's lookup tables (430, 460, 530, 560) can each be considered to comprise a group of n interleaved 1-bit lookup tables, for an n-bit table lookup.

Regarding claims 4 and 5, Cui also shows a "first register" memory (410 or 510) from which data is read out to a "second register" FIFO (480 or 580).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (703) 305-9681. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen M. Baker
Primary Examiner
Art Unit 2133

smb